IMAGING CIRCUIT AND METHOD OF SPATIAL COMPENSATION

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Background of the Invention

The present invention relates in general to semiconductors, and more particularly to integrated imaging circuits.

High resolution imaging systems such as scanners and digital cameras capture images by projecting light from an object through a lens and onto an optical sensor. A low manufacturing cost and low power operation is achieved by fabricating the sensor on a semiconductor die configured with an array of photoactive sensing devices such as charge-coupled devices, photodiodes, or phototransistors. The photoactive devices respond to the light projected from the object by generating proportional pixel signals which are processed through an imaging circuit to produce viewable imaging data.

In most imaging systems, different regions of the sensor have different responses to the light projected from the image. That is, photoactive devices in different regions of the sensor generate pixel signals of different amplitudes even when the light intensity is the same. Such nonuniformities can be caused by semiconductor process variations across the die, aberrations in a focusing lens or by thermal gradients across the sensor. As a result, objectionable shadows are present in portions of the displayed image.

Hence, there is a need for an improved imaging system that can compensate for different responses to light across different regions of an optical sensor.

Brief Description of the Drawings

FIG. 1 illustrates a partially exploded isometric view of an image capturing system in accordance with the present invention; and

FIG. 2 illustrates a processing circuit for pixel signals in accordance with the present invention and

Detailed Description of the Drawings

In the figures, elements having the same reference number have similar functionality.

FIG. 1 illustrates a partially exploded isometric view of a scanner 10 or similar image capturing system, including an image capture device 20, a computer 21 and a display device 22. Scanner 10 captures an image 12 for converting to digital data in a format recognizable for displaying by display device 22, as will be described.

A package 24 houses an imaging integrated circuit 26 having a lid 28 with a transparent portion 30 for transmitting light reflected from image 12. The light is projected onto an optical sensor 32 formed in a region of integrated circuit 26. Optical sensor 32 is formed as an array of photoactive semiconductor devices designated as photodetectors functioning as pixel sensors.

Transparent portion 30 operates as a focusing lens to focus light in a focal plane in which optical sensor 32 is disposed. Alternatively, focusing is achieved with an external lens (not shown) interposed between image 12 and sensor 32. Light projected through transparent portion 30 onto the photodetectors of sensor 32 produces analog pixel signals proportional to the light intensity. In many

systems, imperfections in transparent portion 30 and/or an external lens result in the intensity of light being nonuniformly transmitted across sensor 32. In other systems, nonuniform pixel signals can be generated in different regions 52 of sensor 32 even when the light intensity is the same, due to thermal gradients or process variations across integrated circuit 26. Such an uneven response of the photodetectors produces objectionable shading of portions of a displayed image.

To compensate for this problem, sensor 32 is subdivided into localized regions 52 within which pixel signals of substantially equal amplitudes are generated when equal light intensities are projected on different photodetectors. The physical size of the regions 52 is determined by the variation in the response to light across sensor 32. When the variation is large, sensor 32 is divided into smaller regions 52 to ensure that the photodetectors within a region 52 have substantially equal light responses. Differences in amplitudes of pixel signals generated by photodetectors in different regions 52 are compensated with a signal processing circuit 34 to reduce or eliminate shadowing. The response to light across sensor 32 depends on lens quality, thermal gradients, etc., of scanner 10.

In the embodiment of FIG. 1, scanner 10 is monochromatic, i.e., senses in black and white, and sensor 32 is configured with one row of 2,752 photodetectors disposed in forty-three regions 52. Hence, each region 52 includes sixty-four photodetectors and their associated selection circuitry. When used in a digital camera, sensor 32 typically is implemented as a row/column matrix of photodetectors rather than as a single row.

Note that numerous other configurations are possible for sensor 32. For example, when scanner 10 is configured to capture color images, color filters can be interposed between an image and sensor 32 so that each photodetector responds to light of a particular color. In an RGB system, sensor 32 may include one row of devices responsive to red light, another row responsive to blue light and a third row responsive to green light. Partitioning into regions can occur within or among these rows to obtain the advantages of the present invention whether or not photodetectors responsive to different colors are combined into the same region. If desired, each photoactive device can be disposed in its own region 52, so that processing circuit 34 compensates for sensitivity differences among any of the photodetectors in sensor 32.

Since a given lens design, lighting system, or process variation often has a predictable and systematic type of shading across a die, the partitioning of sensor 32 into regions 52 typically occurs when scanner 10 is being characterized during its development phase. Alternatively, scanner 10 can be configured with calibration circuitry to allow a user to adjust the number of regions as needed.

Signal processing circuit 34 receives user selected starting and ending addresses on a node 45 from computer 21 to define the scan boundaries. These addresses are used to generate address data on conductors 35 and 36 for selecting the photodetectors whose pixel signals are provided on a bus 38. Circuit 34 processes the pixel signals to produce digital imaging data at a wire bond 37 and a lead 39 of package 24. In alternative applications, parallel imaging data is provided on multiple leads and transferred on a bus to computer 21.

Computer 21 is a digital signal processing device programmed to generate the starting and ending scan addresses and to provide control data to circuit 34. Each region 52 of sensor 32 has a corresponding value of control data which is used to compensate for differences in the sensitivity of photodetectors as will be described. Computer 21 also receives the digital imaging data from circuit 34 for formatting and viewing on output device 22. Output device 22 is shown as a monitor, but can be another type of device such as a printer, a storage device such as a disk drive, etc.

FIG. 2 illustrates a schematic diagram of integrated circuit 26 including optical sensor 32 and processing circuit 34. Pixel signals generated by sensor 32 are provided in parallel on bus 38. The pixel signals are selected for converting to a serial stream on a node 65 by a two stage multiplexing circuit. The first multiplexing stage includes a multiplexer 62 for selecting one of forty-three regions 52 of sensor 32. Selection is controlled by address data provided on six bit bus 36 from a pixel address generator 66. Hence, multiplexer 62 has 2,752 inputs coupled to bus 38 and sixty-four outputs coupled to a sixty-four bit bus 71 for providing sixty-four pixel signals generated within a selected region. Multiplexer 62 is implemented as a decoding matrix of analog switching devices such as transmission gates to operate as a one of forty-three analog multiplexer.

The second multiplexing stage includes a one of sixty-four analog multiplexer 63 for selecting from among pixel signals within a region 52 selected by multiplexer 62. Inputs of multiplexer 63 are coupled to bus 71 for receiving the pixel signals and a selected pixel signal is

provided on node 65. Multiplexer 63 includes a matrix of analog switching devices similar to the matrix of multiplexer 62. Pixel signals within a region 52 are selected with address data provided on six bit bus 35 from pixel address generator 66.

Pixel address generator 66 receives the starting and ending addresses from computer 21 on node 45 for setting the boundaries of a scan. Pixel address generator 66 includes one or more programmable counters which are incremented with a system clock SYSCLK to produce the series of binary pixel addresses on buses 35 and 36. The binary pixel addresses are applied to multiplexers 62 and 63 to produce a serial stream of pixel signals on node 65.

A correlated double sampling (CDS) circuit 68 operates as a sample and hold sense amplifier that extracts projected light information from the pixel signals while rejecting system noise. An input is coupled to node 65 to sense the pixel signals to provide a stream of analog sense signals at an output coupled to a node 70. The sample and hold functions are timed from system clock SYSCLK to synchronize with the rate of the pixel signals. Correlated double sampling is a standard method used in imaging circuits to sense pixel signals. Briefly stated, ~~a~~ a selected pixel signal has two portions: a reference (or dark) portion whose amplitude is indicative of a zero light condition, and a signal (or light) portion whose amplitude is indicative of the intensity of the light projected on the photodetector to generate the pixel signal. The reference level is sampled by CDS circuit 68 on one transition of SYSCLK and the signal level is sampled on another SYSCLK transition while holding the reference level. CDS circuit 68 subtracts the reference level from

the signal level and amplifies the difference to produce an analog sense signal on node 70. Hence, analog sense signals contain information regarding the intensity of light projected on corresponding photodetectors.

A programmable gain amplifier (PGA) 72 operates as an analog amplifier whose gain is set with digital CONTROL data received at a control input at a node 74. A signal input is coupled to node 70 to receive the stream of analog sense signals and an output at a node 78 provides an imaging signal stream. PGA 72 amplifies each analog sense signal to a gain whose magnitude is set by the applied value of CONTROL data. Each region 52 has a corresponding value of CONTROL data which typically is set when scanner 10 is characterized 10 during its development phase. Alternative methods of setting CONTROL values can take advantage of the inherent mapping between areas of a displayed image and regions 52 of sensor 32. For example, a user can capture a white image and view it on display device 22 while manually adjusting CONTROL data through a graphics interface to compensate for shadowy areas created by different responses to light of different regions 52.

A memory circuit 76 stores CONTROL data transferred from computer 21 on conductor 43. An output is coupled to node 74 for providing CONTROL data to PGA 72. Note that pixel addresses are applied to memory circuit 76 to retrieve CONTROL data while being applied to multiplexers 62 and 63 to select pixel signals, so the same pixel addresses that control multiplexers 62 and 63 are used to access CONTROL data from memory circuit 76. Therefore, as analog sense signals are amplified through PGA 72, the correct CONTROL data is retrieved from memory circuit 76 on node 74 to dynamically alter the gain of PGA 72 to

compensate for the different sensitivities of regions 52 to light. In effect, altering the gain "on the fly" spatially compensates for these nonuniformities across sensor 32 to produce higher quality displayed images.

The imaging signal stream on node 78 is applied to the input of an analog to digital converter (ADC) 80 for converting to digital imaging data at an output coupled to wire bond 39. Recall that the imaging signal stream is provided at a rate set by SYSCLK. To synchronize with the imaging signal stream, ADC 80 is clocked with SYSCLK to convert the imaging signal stream to digital imaging data as it is received.

By now it should be appreciated that the present invention provides a circuit and method of compensating for a nonuniform response across an optical sensor. The nonuniformity results in pixel signals generated in different regions of the optical sensor having different amplitudes for a given intensity of light. The optical sensor is divided into physical regions small enough to ensure that the photodetectors within each region generate substantially equal pixel signals for the given light intensity. A processing circuit compensates for different responses among different regions with a programmable gain amplifier whose gain is adjusted when the regions in which the pixel signals are generated changes.